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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,301	12/31/2003	Andy H. Gan	X-1294 US	9777

24309 7590 03/21/2007

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
GARBOWSKI, LEIGH M	
ART UNIT	PAPER NUMBER
2825	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/749,301	GAN ET AL.	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1 and 3-13* is/are allowed.

6)☒ Claim(s) *14,18 and 19* is/are rejected.

7)☒ Claim(s) *15-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 14, 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Jenkins [U.S. Patent #7,073,148 B1].

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 14, a method of forming an integrated circuit, comprising: associating a diode circuit with each of a plurality of primary input ports of an embedded logic circuit defining at least a portion of the integrated circuit, a remaining portion of the integrated circuit defining existing logic circuitry [column 3, lines 35-39; column 4, lines 54-59]; laying out components of said logic circuit [column 3, lines 32-33]; routing conductors connecting said components [column 3, lines 32-33]; and integrating said logic circuit with said existing logic circuitry onto a chip to form the integrated circuit [column 3, lines 41-43; column 5, lines 34-35]. As per claim 18, wherein said integrated circuit is a programmable logic device and at least a portion of said existing logic circuitry comprises programmable logic blocks [column 4, lines 54-67]. As per claim 19, wherein said embedded logic circuit is a processor [column 4, lines 54-67].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 14, 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. [U.S. Patent #6,594,809 B2].

Wang et al. teach a method of forming an integrated circuit, comprising: associating a diode circuit with each of a plurality of primary input ports of a logic circuit defining at least a portion of the integrated circuit, a remaining portion of the integrated circuit defining existing logic circuitry (col. 2, line 63 to col. 3, line 6); laying out components of said logic circuit (col. 1, line 33-36); routing conductors connecting said components (col. 1, line 38-49); and integrating said logic circuit with said existing logic circuitry onto a chip to form the integrated circuit (col. 5, line 16-21). However, Wang et al. do not explicitly teach an embedded logic circuit, wherein said integrated circuit is a programmable logic device, comprises programmable logic blocks, or wherein said embedded logic circuit is a processor. It is well-known that standard cells are typically used to implement integrated circuit cores, this is evidenced in applicant's own specification [paragraphs 0023, 0025] which describes standard cells being the basis for programmable logic devices. Wang et al. go on to claim an integrated circuit formed on a semiconductor chip, comprised of a plurality of modules; this description appears to encompass embedded logic circuits save for the explicit use of embedded or programmable. Thus, a person of ordinary skill in the art at the time of the invention would have found it obvious to employ the Wang et al. reference to obviate the claimed invention because "the antenna diode insertion method and related IC described above not only provide for the reliable accomplishment of the objects of [it but] do so in a particularly economical and efficient manner" [column 5, lines 30-33].

Allowable Subject Matter

Claims 1, 3-13 are allowed.

The following is an examiner's statement of reasons for allowance: the prior art of record discloses associating diode circuits with inputs of standard cells and routing conductors for connecting said inputs to said associated diode circuits if it is determined that an input has an antenna rule violation. The subject matter of the independently claimed invention presents that each at least one primary input port is connected to the associated diode circuit regardless of antenna rule violations. Thus, the prior art of record does not disclose, and there is no suggestion therein, automatically inserting antenna diodes for an IC design particularly comprising routing conductors for connecting said components and connecting each said at least one primary input port to said associated diode circuit.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claims 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: although the prior art of record discloses identifying antenna rule violations associated with inputs of an embedded logic circuit, the prior art of record does not disclose, teach, or suggest associating at least one additional diode circuit with said offending primary input port.

Response to Arguments

The applicant argues that Wang does not teach or suggest associating diode circuits with primary input ports of a block; that a primary input port is a top-level input to the embedded block. However, the examiner disagrees. Given that both the reference and applicant's own specification teach that standard cells are part of a library and filler cells are inserted [column 3, lines 53-64; paragraph 0023], the examiner contends that Wang et al. do teach associating diode circuits with inputs of a block. Considering that both the reference and applicant's own specification similarly teach inputs to standard

cells [column 5, line 5; paragraphs 0020, 0021, 0023, 0024], and considering that standard cells are typically used to implement embedded logic designs, it follows that these inputs are by definition primary inputs as defined by applicant. See also the similarity between Wang et al. figure 4 and applicant's own figure 2. It appears to the examiner that even though certain terms are not explicitly recited, the concepts of the subject matter disclosed by the applicant and taught by Wang et al. are rather equivalent. Therefore, given a broadest reasonable interpretation of the claimed subject matter, the examiner maintains that Wang et al. obviates the claimed invention.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lee et al. [U.S. Patent #6,502,229 B2] disclose inserting antenna diodes into an IC design, including standard cells [column 3, lines 56-63; column 6, lines 33-51] and input nodes [column 5, lines 8-20; column 7, lines 14-15.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LEIGH M. GARBOWSKI
PRIMARY EXAMINER